PCT

WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 3 :
H04B 3/23; H04L 25/03

A1

(11) International Publication Number: WO 83/01876

(43) International Publication Date: 26 May 1983 (26.05.83)

(21) International Application Number: PCT/GB82/00329

(22) International Filing Date: 18 November 1982 (18.11.82)

(31) Priority Application Number: 8134898

(32) Priority Date: 19 November 1981 (19.11.81)

(33) Priority Country: GB

(71) Applicant (*for all designated States except US*): INTERNATIONAL STANDARD ELECTRIC CORPORATION [US/US]; 320 Park Avenue, New York, NY 10022 (US).

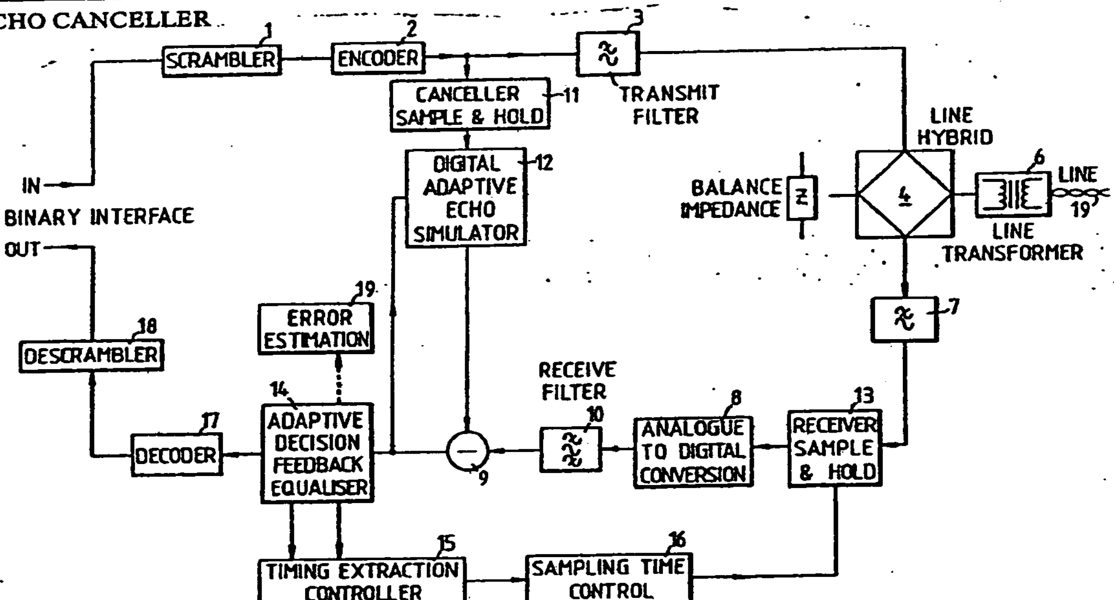
(72) Inventor; and
(75) Inventor/Applicant (*for US only*) : FISHER, David, Anthony [GB/GB]; 71 Little Warden, Saffron Walden, Essex (GB).

(74) Agent: CAPSEY, Sydney, Ross; STC Patent Department, Edinburgh Way, Harlow, Essex CM20 2SH (GB).

(81) Designated States: AT (European patent), BE (European patent), CH (European patent), DE (European patent), FR (European patent), GB (European patent), JP, LU (European patent), NL (European patent), SE (European patent), US.

Published
With international search report.
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

(54) Title: ECHO CANCELLER



(57) Abstract

In a fully digital telephone system in which the subscriber to exchange loops are of the twisted pair type it is necessary to be able to convey PCM in either one of two directions. To do this it is necessary to cancel the interference being caused by imperfections in the hybrid (4). This interference is removed by applying a defined fraction of the outgoing signal from the encoder (2) in the GO path via a sample and hold circuit (11) and an echo simulator (12). The latter includes coefficient generating circuits controlled by the signal in the RETURN path and by the outgoing signal. These coefficients are subtracted from the RETURN path signal to substantially eliminate this interference. Intersymbol interference is eliminated by a feedback equaliser (14) which controls the sample and hold circuit (13) in the RETURN path to force to zero an adaptable weighted sum of symbol spaced estimates of the overall transmitted symbol time response from the transmitter to detector, specifically shaped by both analogue and digital filters.

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AT	Austria	LI	Liechtenstein
AU	Australia	LK	Sri Lanka
BE	Belgium	LU	Luxembourg
BR	Brazil	MC	Monaco
CF	Central African Republic	MG	Madagascar
CG	Congo	MR	Mauritania
CH	Switzerland	MW	Malawi
CM	Cameroon	NL	Netherlands
DE	Germany, Federal Republic of	NO	Norway
DK	Denmark	RO	Romania
FI	Finland	SE	Sweden
FR	France	SN	Senegal
GA	Gabon	SU	Soviet Union
GB	United Kingdom	TD	Chad
HU	Hungary	TG	Togo
JP	Japan	US	United States of America
KP	Democratic People's Republic of Korea		

ECHO CANCELLER

This invention relates to a digital transmission system in which digital data information such as PCM is conveyed in either one of two directions over a single transmission path.

In such a system the stations at the end of the transmission path each have a GO and RETURN path, these paths being coupled to the transmission path via a hybrid or its electronic equivalent. The transmission path may be a two-wire twisted-pair which would normally be one of a number of such pairs in a cable. Unfortunately imperfections in the hybrid or its equivalent cause an unwanted signal to find its way from the GO to the RETURN path, and it is an object of this invention to provide for a substantial reduction in or elimination of this unwanted signal.

According to the present invention there is provided a digital transmission station for use in a system in which digital information such as PCM is conveyed in either one of two directions over a single transmission path, wherein the station includes GO and RETURN paths coupled to the transmission path via a hybrid or its equivalent, wherein in the RETURN path the received information is applied to an analogue-to-digital converter which produces one output per received symbol which output has a digital format and represents the signal value at a specific sampling instant, wherein said output is applied via a

digital filter of response $(1-Z^{-1})$ to one input of a subtractor circuit, the information thus applied to said one input of the subtractor circuit including, due to imperfections in the hybrid or its equivalent, an unwanted signal, and wherein a sample and hold circuit receives its input from the GO path and its output is applied via an echo simulator to another input of the subtractor circuit, so that the latter subtracts from the information in the return path a version of the signal in the GO path, whereby the output from the subtractor is a version of a received signal from which the unwanted signal has been substantially removed.

Thus this arrangement involves the use of digital signal processing techniques to achieve full duplex transmission of digital information, in the present case PCM, on a single pair of a multiple twisted-pair cable, in particular 144 kbt/s on exchange to subscriber loops. To simplify the system, the processing operations are performed at the line symbol rate and to minimise both near-end and far-end cross-talk, and also noise sensitivity, the non-linear process of decision feedback equalisation (DFE) is used.

Embodiments of the invention will now be described with reference to the accompanying drawings, in which Fig. 1 is a digital transmission station embodying the invention.

Fig. 2 is a functional diagram of an echo canceller arrangement usable to connect the scrambler and the subtractor in Fig. 1.

Fig. 3 is a functional diagram of an adaptive decision feedback equaliser (ADFE) usable in Fig.1.

Fig. 4 is a functional diagram of an ADFE, similar to that of Fig. 3 but with transient and lock up protection.

Fig. 5 is a graph of channel impulse response,

useful in explaining the invention.

Fig. 6 is a functional diagram of an ADPE with means to generate a timing extraction control signal.

Fig. 7 is a diagram explanatory of sample and hold control at a slave end.

Fig. 8 shows sampling phase clock diagrams.

Fig. 9 is a functional diagram of an echo canceller with transferable coefficients.

In a system using the present invention there are two ends, the master end being the one with a master oscillator which controls the PCM transmission rate, the other or slave end being synchronised to the master end by a clock synchronisation circuit. The two ends differ because of the clock extraction and sampling time adjustment needs, but the system operates at each end substantially as will be described with reference to Fig. 1, which shows schematically the component parts of one end of the echo cancelling transmission system.

The binary data to be transmitted in the GO path is initially scrambled by a scrambler 1 to eliminate auto-correlation in the transmitted data and correlation between in the two directions of tranmission. In a binary system, the encoder 2 to which the output of the scrambler 1 is applied is a differential encoder. This gives a binary output at the same rate as the input, such that the output changes when the input is 1 and does not change when the input is 0. The encoded information is applied to a transmit filter 3 to reduce high frequency energy sent to the cable at frequencies greater than half the symbol rate. This filter can be a first order low pass filter with 3dB attenuation at the system's bit rate. The line hybrid 4 couples the output from the filter 3, which is the transmit signal, to the line, and presents a resistive impedance to the

line of 140 ohms.

On the RETURN side there is a filter 7 which precedes an analogue-to-digital converter 8, which filter limits the spectrum of the received data to the half bit rate. It can be a third order Butterworth filter with attenuation of - 6dB at the half digit rate. The converter converts the signal from the line into a form more suitable for processing in the rest of the RETURN path.

The received signal comprises the wanted far end signal, plus unwanted local signal due to the imperfect loss of the hybrid 4. The impulse response from the GO path to the echo canceller subtractor 9 is referred to as the trans-hybrid impulse response. The output of the converter 8 is applied to a digital filter 10 whose parameters depend on the way timing extraction is implemented, but in a simple case the filter 10 has the response $1-z^{-1}$.

The GO and RETURN paths are coupled by a sample and hold circuit 11 and a digital adaptive echo simulator 12. This simulator is an adaptive transversal filter which adjusts automatically to match the transhybrid impulse response until the difference signal from the subtractor 9 has substantially no local signal content. It generates one output for each sampled input value from the sample and hold circuit 13. The simulator 12 operates on the data to be sent, which is gated into it according to the method of timing extraction. Note the output from the subtractor 9 to the simulator 12.

The output from the subtractor 9 is also applied to an adaptive decision feedback equaliser (ADFE) 14, whose purpose is to detect the received symbol values and to remove inter-symbol interference (ISI) between received symbols due to the transmission through the cable. The equaliser also controls the timing due to its constant estimation of the channel

impulse response, see below. This ADFE can be similar in principle to that of our Application No. 8032249 (D.A. Fisher 2). The output of this ADFE is applied to a timing extraction controller 15, which via a sampling time control circuit 16 controls the sample and hold circuit 13.

The output of the ADFE 14 is also applied to a decoder 17, which is in effect the inverse of the encoder 2, the output from which passes to a descrambler 18 the output of which is the RETURN signal output. Also associated with the decoder 17 is an error estimation circuit 19.

In considering the line codes used, a distinction is drawn between the number of levels seen at the receiving detector point, and a two level system will be described, followed by an indication of the modification needed for a three level system.

Fig. 2 shows the echo canceller, which includes the echo simulator (12, Fig.1), which is fed by the sample and hold circuit 11 and which feeds the subtractor 9 at which echo cancellation takes place.

Let the transhybrid impulse response (TIR) be g(t) and the sampled transhybrid response G_i. With a transmitted impulse sequence T_i, the hybrid output consists of the convolution of the transmitted symbols with the TIR, plus the far-end transmission F_i and an external noise component N_i.

$$R_i = \sum_{j=0}^{\infty} G_j T_{i-j} + F_i + N_i \qquad (1)$$

The echo simulator (12, Fig. 1) is an adaptive transversal filter having ($\underline{m}$ + 1) coefficients, and consists of $\underline{m}$ symbol delay elements such as 21, 22, and ($\underline{m}$ + 1) accumulators formed by the elements 23, 24, 25 which store the coefficient values, with two multipliers such as <u>ma</u>(1) and <u>mu</u>(1) per coefficient. The current transmitted symbol value

T_i and the previous m transmitted symbol values are multiplied by the accumulator values K_i using the multipliers mu(1) to mu(m) to form an estimate of the transhybrid signal component of the signal Z_i.

$$Z_i = \sum_{j=o}^{m} K_j T_{i-j} \qquad (2)$$

The difference signal between the sampled input signal R_i and the echo simulator estimate Z_i is S_i :

$$S_i = R_i - Z_i$$

$$\sum_{j=o}^{m} T_{i-j} (G_j - K_j) + \sum_{m+1}^{\infty} G_j T_{i-j}$$

$$+ F_i + N_i$$

The difference signal derived from the output of the subtractor 9, is scaled by a factor $^1/C$, in an error scaler 27, and used to increment each accumulator after correlations with the corresponding symbol value using multipliers ma(1) to ma(m). The new coefficient value K_n is then

$$K_n = K_n + \frac{S_i}{C} \cdot T_i - n \qquad (4)$$

Thus the output (a) being the difference signal (Si) between the echo simulator output Zi and the received sampled input values Ri in the RETURN path, goes to the equaliser (14, Fig.1).

The system is based on an ADFE, Fig.3 operating on the echo cancelled output which is samples spaced by one symbol period. In describing this equaliser we assume that any content of the local

signal superimposed on the wanted far-end signal is totally removed by the echo canceller.

The function of the ADFE is to remove ISI at the decision point by subtraction just before the decision point. Fig. 3 represents the operation of the ADFE. The impulse responses (TIR) must have a rise time to maximum or near maximum value at most equal to the time between successive transmitted symbols. The first clearly-defined maximum of the impulse response for a given set of symbol spaced samples is called the cursor value of the response. The channel is assumed to be linear in that the superposition principle applies throughout from transmitter to receiver. Note that the sequence-dependent equalisation may be used to overcome certain types of non-linearity. It is also assumed that after a finite time, the summation of all unsigned values of the impulse response is finite and less than the cursor value, such that a finite length equaliser may be used.

We now describe the operation of the equaliser, Fig. 3. The sampled input signal S_i has subtracted from it by a subtractor 30 an estimate of the ISI at that sample time formed by summating the ISI due to previous symbols. The $\underline{n}$th constituent of the sum, produced by the summator 31, is formed by the product of the $\underline{n}$th previous decision value, and the $\underline{n}$th post cursor unit symbol time response estimate. The decision value from the current sample is D_i, that for the $\underline{n}$th previous sample is D_{i-n}, and the estimated value of the unit symbol time response at time $\underline{t}$ due to a symbol received at $\underline{t}_{i-n}$ is C_n. This estimate is the coefficient value, so the estimate of ISI due to each previously received symbol at $\underline{t}_{i-n}$ is $D_{i-n}\ C_n$.

The sampled value free of estimated post cursor ISI is passed to the threshold detector 32,

which determines the symbol value. The value on which the decision due to the sample S_i is made is thus

$$d_i = S_i - \sum_{n=1}^{m} D_{i-n} C_n \qquad (5)$$

The decision value (D_i) is then multiplied using element 35 by a cursor coefficient estimate C_o, which is the value of the accumulator element 34. This product is then subtracted by a subtractor 37 from the value at the input of the detector 32, and is termed the error value. Thus the error value is formed by the following calculation :

$$e_i = S_i - \sum_{n=o}^{m} D_{i-n} C_n \qquad (6)$$

The error estimate is used to update the coefficient values C_o to C_n. Each coefficient is then incremented by the product of the error value scaled by element 36 and the symbol value used to form the product with that coefficient in deriving the error value. Thus the new value of the n th coefficient C_n^1 becomes

$$C_n^1 = C + \frac{ei}{\lambda} \cdot D_{i-n} \qquad (7)$$

The next sample is taken and all previous detected symbols shifted one cell through the memory. Such an equaliser is described in more detail in our above-mentioned Application No. 8032249 (D.A. Fisher 2)

There are two more features of the ADFE, one being the provision of transient and lock-up protection while the other generates a signal for sampling time control, and Fig. 4 shows additions to the ADFE for disabling the coefficient values when a large transient is detected at the input, and for detecting the state which can occur when the equaliser is in a stable but invalid operating state.

A weighted running mean W_m is produced by the subtractor 30, scaling circuit 40 and accumulator 41. The coefficient updating is disabled for F3 symbols, via a threshold detector 42 if the ratio of the magnitude of the input sample value to the mean value $S_i\ /W_m$ exceeds F1. The weighted running mean W_m is also used to detect lock-up by comparison in a threshold device 43 with the value of the ADFE cursor value C_o, which is always positive. If the ratio of $^{Co}/Wm > F2$, the coefficients are set to zero as can be seen in Fig. 4.

With binary and ternary systems a preferred set of values is F1 = 2, F2 = 2 and F3 = 4.

We now consider timing extracting. The slave end extraction is controlled by defining specific ratios between symbol spaced values of the overall transmission impulse response between the transmitter and receiver. The sampling time is adjusted until these conditions are met. The required correlation ratios may be varied according to other criteria to maintain an optimum sampling instant under differing conditions. The absolute value of the weighted running mean W_m is used for this purpose.

Consider the impulse response defined in Fig.5 curve 'a' as seen at the input to the equaliser 14, Fig.1. This is due to the transmitter pulse shaping, the transmit filter 3, Fig. 1, transmission through the line hybrid, 4, transmission through the line transformers and cable and the low-pass band-limiting filter 7. The analogue to digital conversion is in this case assumed to give a true sample of the instantaneous signal value as a number. The digital filter 10, Fig.1 is not included. Given such an inpulse response a discriminator characteristic may be obtained from the continuous estimates of the channel impulse response available within the ADFE. The dicriminator characteristic may be obtained by a

combination of operations on the coefficient estimates and on the signal itself.

For the channel response of curve a, Fig. 5, the system diagram of Fig. 6 defines the operations needed to derive a signal to control a phase locked loop directly from the coefficients. Fig. 6 relates to the ADFE with means to produce an estimate of a control signal generated for timing extraction control. Here the time constants for control of the sampling control loop may be chosen separately from the integration constants of the equaliser proper.

The function of the system of Fig. 6 is to produce the value $\alpha h(o) + \beta h(1)$ and the signal is then used to control a phase-locked loop or a switched phase adjustment, as described below.

The basic structure and operation of the ADFE is as described above, see Fig. 3. The two values needed in this case are referred to as independent estimates of the cursor value and the first post-cursor value. Each is formed as follows. The error signal e_i which comes from the subtractor 37 is the remainder of the sampled input signal after the cursor and all post-cursor estimates of the sequence of transmitted symbols convolved with the transmission channel have been removed.

An estimate of the value of the cursor coefficient C_o is formed by the loop consisting of the symbol value and coefficient accumulator multiplier 35, the subtraction of the cursor content of the signal by the subtractor 37, the scaling function 36, and the correlation formed by the multiplier and accumulator 33, 34. However, the loop integration time is controlled by the value of λ which is the loop gain.

To generate an estimate free from this constraint the value D_i times C_o is added back into the error signal e_i and the product of this

modified remainder with the appropriate decision value is used for timing control. This is called a modified channel estimate, M(n) corresponding to the channel impulse response h(t=n) being n symbol periods after the decision point. Independent estimates of any post-cursor value may similarly be obtained. These may then be scaled and added or subtracted to give the control signal. The coefficients themselves may be directly used if the inherent integration time constants defined by λ are suitable.

Referring to the channel response curve a, Fig.5, this is typical of those encountered on twisted-pair transmission lines as used in the local telephone subscriber network. If the sampling time is adjusted until the difference between the channel impulse response estimate at h(t=o) and h(t=1) (t relative to the decision point) is zero, then the value of C_o (being the equaliser estimate of the channel impulse response at the decision time) is near the first peak of the impulse. The conditions previously mentioned for correct operation of the ADFE are then satisfied. The difference between samples taken at unit symbol intervals as the sampling time is varied is given by curve b of Fig.5. Note that for this channel response, h(t)-h(t+1) is free from inflexion for a third of a symbol period either side of the zero crossing and thus provides a clean signal for timing control.

An alternative giving the same sampling time as forcing the estimate of h(t=O) -h(t=1) to zero is to place a digital filter with response $(1-z^{1})$ in the signal path, e.g. in position 10, Fig.1, constructed by a symbol period delay element and a subtractor. Then the result on the overall transmission impulse response Fig.5, curve 'a' is as given in Fig. 5 curve 'b'. In this case the forcing of h(t=1) to zero alone can be used to control the timing circuits.

A preferred implementation of this method of timing extraction uses both digital filtering of the channel and a switched operation on the estimates of h(t=0) and h(t=1) to generate the timing loop control signal. The filter 7, Fig. 1 in this implementation is specifically $1-Z^{-1}$ and the weighted running mean is used as a switch to control whether the h(t=1) estimate alone or 2h(t=0) + 3h(t=1) is used (for short cables) to control the sampling times. Hysteresis is added to the switch acting on W_m by having a higher threshold for switching from the 2h(t=0) + 3h(t=1) controlled state to the h(t=1) controlled state than in the opposite direction. A particular feature of this operation is that it introduces no discontinuity in correct operation of the system.

Four methods of application of the timing control signal generated by one of the methods described above to control the receiver sampling time are described. The function of these methods is to so alter the receiver sampling time that a predetermined weighted sum of the channel response estimates is reduced to zero. At the slave end the transmit time tracks the sampling time so that the coefficients of the echo simulator remain constant as the sampling time is changed.

The most general system is given in Fig. 7. Here a weighted sum of the channel estimates M(0) to M(n) is formed which is to be zero-forced. The use of a signal (X) to control the coefficients of the weighted sum either continuously or in steps enables the system to be adapted to suit different channel characteristics. Thus both the values previously defined as W_m and C_o are indicators of the magnitude of the signal which for a cable may be used to adjust to a predictable sampling time optimum. In addition to adjusting the actual sampling time instant, the loop gain of the phase-locked loop may

also be adjusted to compensate for a reduced input signal amplitude. This uses element 70, which generates an inverse proportionality function, and by increasing the output of the weighted summation in inverse proportion to the signal magnitude indicator X. The lossy integrator 72, 73, 74, with integration scaling constant γ, provides a steady control voltage for the VCO 75 after the digital to analogue conversion.

In a second implementation the coefficient estimates available from the accumulator outputs are used directly. The function

$$f(A^*C_o + B^*C, +C^*C_2 + \ldots)$$ is performed digitally and the sign of the result used directly to control the VCO such that if the sign is +ve then the VCO is set to its maximum frequency, while if the sign is -ve the VCO is set to its minimum frequency. In this implementation which gives a first order control loop, the VCO range must be limited. The system operates satisfactorily with an oscillator range of up to $\pm$ 1000 parts per million.

In a third implementation the modified channel estimates M(n) as defined above are used. The predetermined function

$$F(A^*M(O) + B^*M(1) + C^*M(2) + \ldots.)$$

is performed digitally and the sign of the result is used to interface to analogue circuitry. An analogue integrator then precedes the VCO, the time constants of the integrator and VCO being chosen to match the system requirements.

A fourth implementation of the slave end timing control uses a digital phase locked loop, and the circuit is similar to that to be described for the master end timing extraction. The difference is that the canceller sample and hold, the receiver sample and hold and the transmitter symbol clock are all operated in synchronism and the phase of all three are

simultaneously advanced or retarded in small steps with respect to a fixed crystal oscillator reference clock nominally of frequency equal to the master clock at the master end. The following description may thus be applied to the slave end by considering these three synchronous clocks to be controlled from the receiver sampling clock. Further by virtue of the echo canceller being in synchronism with the receiver sampling clock, transferable echo canceller coefficients are not required, and the waiting period between phase steps can be shortened.

The master end of the system is the end with the reference clock, which for an exchange to subscriber loop is the exchange end. The control signals used may be derived as described above. Only the sign of the resultant signal is important, as the adjustment is a single step forwards or backwards in time with respect to the nominal symbol interval. Referring to Fig. 8 at the master end the transmitter clock is locked to the local clock reference and the sample instruction is adjusted in small steps, there being S steps in a symbol period.

To enable a continuous incremental advance or retardation of the sampling time with respect to one symbol interval, a "fold-around" technique is used in the controlling circuitry. At the master end this involves an alteration to the echo canceller so that at the "fold-around" boundary there is no discontinuity of operation. Operation of the timing may be explained with reference to Figs. 8 and 9.

The sampling time is adjusted with respect to a reference point, which is the local reference clock figure 8(a). The sampling time can only change by one step at a time, and two methods which limit the frequency with which steps can occur and which allow the canceller coefficients to adapt to the new sampling time and consequent change in the sampled

trans-hybrid symbol impulse response are described. The step size is a fraction of a symbol period so that the change in the trans-hybrid impulse response is limited and does not cause an error.

The symbol transmit clock is split into S steps such that the receiver sample and hold clock is adjustable to any position between 0 and S-1 by the control circuitry. The receiver sampling time is controlled from a register which defines the current position of the sampling time in terms of the number of steps from the transmit symbol clock; this phase register value corresponds to the receiver sampling phase. Sampling phase 0 corresponds to no time difference between the local clock reference and the receiver sampling clock. In Fig. 8, the local clock reference is defined in Fig. 8(a), and all other clocks are referred to this reference. For s=8, the phase register values are defined in Fig. 8(d). Fig. 8(e) defines the relationship between the local clock reference and the receiver sampling clocks when the receiver sampling phase is 2 and the number of steps (S) = 8. The 0 to 1 transition of the clock is taken to be the edge upon which data is moved into and out of the clocked device.

When the receiver timing control requires the sampling time to be advanced, the sampling phase controlling register content is reduced by one. If the sampling phase is at position 0, the register value and corresponding sampling phase is changed to value S-1. The timing diagram for the change is given in Fig. 8(f) and it is important to note that two receiver samples occur during the transmission cycle 2.

When the receiver timing control needs the sampling time to be retarded the content of the sampling phase control register, and thus the corresponding sampling phase is increased by one. If this phase is at S-1, the phase register value is

changed from S-1 to 0. The timing diagram for the change is given in Fig. 8(g); note that in this transition the change in sampling time omits the sample at sampling phase 0 in the transmission cycle immediately following the S-1 sample. This causes the complete omission from this transmit clock cycle (cycle 3 in Fig. 8(g)) of a receiver sample.

To limit the frequency of the step change in sampling time, we describe two methods. As stated above, only the sign of the timing control signal is used to adjust the digital phase locked loop, this signal being subject to change after each symbol period.

The first method of limiting the step frequency is to latch the phase register every pth symbol, depending on the sign of the control signal. In the second method, the control signal is fed to an up/down counter which is incremented or decremented during each symbol period. When the up/down counter reaches its limit L and is further incremented, it is reset to zero and increments the phase register. Conversely when the up/down counter is at value zero and is further decremented, the phase register is then decremented, and the up/down counter is set to value L.

The echo canceller sample and hold clock is also controlled by the sampling phase circuitry. As the echo simulating filter is an adaptive transversal filter operating on the transmitted data, its output, is synchronous with the receiver sample and hold clock. In Figs. 8(f) and 8(g) it may be seen that there is a slip between the transmitted data and the receiver sample time such that if the receiver sample and hold clock is used to clock data into the echo canceller, a discontinuity of operation would occur when the sampling phase changes from 0 to S-1 and vice-versa. This is overcome by altering the echo simulator as shown in Fig. 9.

The simulation filter is altered in two ways. Firstly the accumulators are linked so that the coefficient values may be shifted forward or backward. Secondly, the clocking of the transmitted data into the symbol shift register prior to multiplication by the accumulator values may be altered to allow for the receiver timing phase changes across the 0 to S-1 boundary and vice-versa.

The sequence of operation for an advance in sampling time corresponding to a change in the sampling phase register value from 0 to S-1 is as follows. The symbol shift register is not clocked. The multiplexers 90, 91, 92 steering the coefficient values are set to the advance state "A" so that the coefficient value operated on by the input data is shifted back one position through the adaptive filter. The sum of products is formed in the usual way as explained above, using the summator 93 and the algorithm presented. Following the updating, the multiplexers are returned to the normal state ("N") and operation continues as above. The net result of this cycle has been to transfer the coefficients back through the adaptive filter by one position.

The sequence of operation for a retard transition in sampling time from a sampling phase S-1 to a sampling phase 0 is as follows. The symbol shift register 94-95-96 is clocked twice. The first symbol register clock pulse is timed to coincide with sampling pulse 0 immediately following the transmit clock which is specifically not used to clock the receiver sample and hold as previously mentioned. This is shown dotted in Fig. 8(g). The second shift register pulse is generated at the same time as the receiver sampling time.

A preferred implementation of the digital phase locked loop in particular where the number of steps (S) and the capacity (L) of the prescaling

up/down counter are integral powers of 2, is to use an up/down counter of length $\log_2 (L+S) = [s + 1]$ as a combined phase register and prescaler. $\mathrm{Log}_2^{(x)}$ is defined as the logarithm to the base 2 of x. The S most significant bits of the up/down counter thus represent the phase register value and the remaining least significant bits form the prescaling accumulator. During each symbol period the up/down counter is incremented or decremented depending on the sign of the timing control signal derived directly from the coefficient values using the preferred ratios described above. A suitable value for the number of steps S at both slave and master ends is 128 (s=6); at the master end a value of L of 256 gives satisfactory operation whilst at the slave end the value of L=128 (l=6) gives satisfactory operation whilst enabling a maximum offset between the local clock references at the slave and master ends of $\pm 10^6/(L*S) = (\pm 61)$ parts per million.

On the local reference clock (LRC) edge a down counter which has previously been loaded to the value of the phase register commences counting down to zero at a rate S times the LRC; the LRC being derived from an exact sub-multiple of the S clock.

On reaching zero the down counter outputs a pulse which is used as the receiver sample clock. This pulse is also used to automatically reset the down counter to the value stored in the phase register. The system is designed so that it will ignore any commence count instruction from the LRC which occurs less than two S clock intervals after the down counter reaches zero.

We now consider the extension of the system to enable transmission and detection of ternary data, as follows. The preferred code encodes 3 binary digits as two ternary digits (3B2T). The code word table is defined below.

BINARY WORD	TERNARY WORD	BINARY WORD	TERNARY WORD
0 000	00	4 100	12
1 001	01	5 101	20
2 010	02	6 110	21
3 011	10	7 111	22

The ternary code word 11 is not used, which enables code word synchronisation by recognition of the word violation 11. For a data format in 18 bit frames, the ternary frame size is 12 symbols. A method of frame synchronisation is used for which at every 8 th ternary frame, the ternary word 1111 is added, which enables frame synchronisation. A second implementation is the addition of the 111 ternary code word every sixth ternary frame. The increase in ternary symbol rate in both cases is 100/96.

A preferred method of transmission is to use transmission potentials of -V,0 and +V volts, corresponding to the ternary symbol values 0,1 and 2 respectively. Operation of the echo canceller is exactly as previously described the symbol registers however containing three level symbol values -1,0 and +1. The decision feedback equaliser operation is similarly altered. In addition a three level detection process is employed in which the comparator function defined in Fig. 3 is expanded to cater for the ternary transmission code as follows :

Input value	Output ternary symbol value
$X > C(O)/2$	+1
$-C(O)/2 < X < C(O)/2$	0
$X < C(O)/2$	-1

Two methods for monitoring the in-servive system error rate without introducing additional code redundancy are described which may be used separately or in combination. The first method is only applicable to the ternary system or a similrly coded system, the

important property of which is the use of a restricted set of code words in which the occurrence of certain code words may be seen to be a code violation. In the case of the 3B2T code described, the code word 11 is used for word synchronisation. Thus once word synchronisation has been achieved the occurrence of the code word 11, except as part of the frame synchronisation word 1111 may be interpreted as an error indicator, and the frequency of this violation used as a measure of error rate. The confidence limit to which an error rate may be measured using this approach depends on the ratio of word violations to the permitted symbol sequence 11 which may straddle two code words and is used for word synchronisation. As this limit is approached the word synchronisation may at a particular threshold be considered lost, and thus operate an alarm if not regained. In this system, the inability to define word synchronisation as described above may also be used to reset the coefficients of the echo canceller and the equaliser adaptive filters to zero, interpreting the word synchronisation loss as the result of system lock-up.

The second method of error detection uses the estimation of the eye height given by the coefficient C_o and the error estimate e defined in the equaliser description in the preceeding text, both of which are available and updated for each symbol received. The difference signal between the magnitude of C_o and the magnitude of a scaled value of the error signal may be used as an indicator of the error rate of the system. Thus if the following expression is negative a 1 is output, if positive a 0 is output.

$$C_o - k*e_i$$

A similar scheme has been described in Application No. 8032249 (D.A. Fisher -2) for the

control of receiver sampling phase. In the case of the system described above, the value of scaling constant $k = 1$ yields close to a one-to-one ratio of error perceived to true symbol error. The estimate of error rate for the case $k = 1$ is thus obtained by counting the number of 1's output from the difference calculating circuit. An alarm signal is enabled when the total exceeds an acceptable level. A continuous method of doing this is to use an up/down counter which is incremented for every perceived error, and decremented every Gth symbol. To detect a perceived error rate exceeding the inverse of G, a threshold on the up/down counter is set which if exceeded causes an alarm signal to be activated. The higher the threshold is set the longer the period the error rate defined by G must be sustained before the alarm is given, thus giving an temporal averaging mechanism. A more immediate and complex extension of the same principle is to set the error scaling (k) in the (C_o-K*e_i)calculation greater than unity. This results in a more frequent negative result being output, each count representing a certain fraction of an error which is dependent on the value of k and on the error statistics. An averaging and alarm system using an up/down counter as described above, the decrementation interval G and the alarm threshold being chosen subject to the required system error performance. It is to be noted that throughout this text the symbol * represents multiplication.

An alternative measure of system performance may be obtained by calculating the running mean of the difference in magnitudes between the cursor coefficient value and the error signal e_i, which gives an absolute measure of the mean margin against noise.

CLAIMS :

1. A digital transmission station for use in a system in which digital information such as PCM is conveyed in either one of two directions over a single transmission path, wherein the station includes GO and RETURN paths coupled to the transmission path via a hybrid or its equivalent, wherein in the RETURN path the received information is applied to an analogue-to-digital converter which produces one output per received symbol which output has a digital format and represents the signal value at a specific sampling instant, wherein said output is applied via a digital filter of response $(1-Z^{-1})$ to one input of a subtractor circuit, the information thus applied to said one input of the subtractor circuit including, due to imperfections in the hybrid or its equivalent, an unwanted signal, and wherein a sample and hold circuit receives its input from the GO path and its output is applied via an echo simulator to another input of the subtractor circuit, so that the latter subtracts from the information in the return path a version of the signal in the GO path, whereby the output from the subtractor is a version of a received signal from which the unwanted signal has been substantially removed.

2. A station as claimed in claim 1, wherein the signal which forms the output from the subtractor circuit is applied to an adaptive decision feedback equaliser to eliminate intersymbol interference and for symbol detection, wherein the equaliser also controls the sampling time or the equivalent thereof of the analogue-to-digital converter, such as to force to zero an adaptable weighted sum of symbol spaced estimates of the overall symbol time response from remote transmitter to local symbol detection, and wherein the received signal is band limited by an analogue filter but shaped by digital filters such

that in combination with the said weighted sum of symbol-spaced estimates the adaptive decision feedback equaliser is operating free from error and is dynamically stable in synchronism with the remote transmitter.

3. A digital transmission station for use in a system in which digital information such as PCM is conveyed in either one of two directions over a single transmission path, wherein the station includes GO and RETURN paths coupled to the transmission path via a hybrid or its equivalent, wherein in the GO path the information is encoded either differentially in a binary system or differentially and then to a random ternary code having provision for word and framing synchronisation, wherein in the RETURN path the received information is applied to an analogue to digital converter with an adjustable sampling time or equivalent, the output from said converter being a digital representation, wherein the output from said converter is applied via a digital filter for symbol shaping to one input of a subtraction circuit, wherein the information thus applied to said one input includes, due to imperfections in the hybrid or its equivalent an unwanted signal, wherein the output of said encoder in the GO path is also applied via an echo simulator to another input of the subtraction circuit in the RETURN path a version of the signal in the GO path, wherein the output of subtraction circuit is so applied to the echo simulator that the amplitude of the input to the subtraction circuit from the echo simulator is so adjusted that the output from the subtraction circuit is the information in the RETURN path with the unwanted signal substantially eliminated therefrom, wherein the output of the subtraction circuit is also applied to an adaptive decision feedback equaliser whose output is applied to a decoder, wherein the decoder performs the inverse

operations to that performed by the encoder in the GO path, wherein the output of the decoder is applied to a descrambler whose output provides the RETURN path information output, and wherein an output derived from the equaliser is used to control timing extraction circuitry so as to control the sampling time or its equivalent of the analogue-to-digital converter in the RETURN path.

4. A station as claimed in claim 3, wherein the echo simulator includes a plurality of coefficient generators to which the output of the encoder is applied via a sample and hold circuit, the application to the first of said generators being with zero delay, the application to the second generator being via one bit time delay, that to the third generator being via two bit times delay, and so on, and wherein the outputs of said generators are summated in a summator whose output is the output of the echo simulator.

5. A station as claimed in claim 4, wherein each said coefficient generator includes a first multiplier to one input of which is fed the local transmitted symbols from the sample and hold circuit, either direct or via the appropriate one of said delays, wherein the other input of each said generator is the output of the subtraction circuit which is applied to it via a scaling factor, wherein the output of a said first multiplier, wherein to the other input of a said second multiplier there is applied the output of the transmitted symbol sample and hold circuit, either direct or via the appropriate one of said delays, and wherein the output of all of said second multipliers are applied to said summator.

6. A station as claimed in claim 3, 4 or 5, and wherein the feedback equaliser includes a further subtraction circuit to one input of which is applied the output of said first-mentioned subtraction circuit, a threshold detector to which the output of said

further subtraction circuit is applied, the output of the threshold detector being applied to the decoder, a number of coefficient generators to which the output of said threshold detector is applied via delays of respectively one, two, three, etc. bit times, and a summator which summates the output of all the said coefficient generators and applies the summated output to the other input of said further subtraction circuit, so that the output of the further subtraction circuit is the RETURN path information substantially free of intersymbol interference.

7. A station as claimed in claim 6, and wherein each of the coefficient generators in the feedback equaliser includes a first multiplier one input of which is fed from the threshold detector via the appropriate one of said delays and the other input is an error estimate applied to it via a scaling factor dependent on the equaliser system loop gain, wherein the output of a said first multiplier is applied to an accumulator whose output is applied to one input of a second multiplier, wherein to the other input of said second multiplier there is applied the output of the threshold detector via the appropriate one of said delays, and wherein the outputs of all of said second multipliers are applied to said summator.

8. A station as claimed in claim 5 or 6, wherein for transient limitation and lock-up protection a weighted running mean of the output of the first-mentioned subtraction circuit is made by feeding a signal representative of the magnitude of the subtraction circuit output to an input to a further subtraction circuit, wherein the output of the accumulator is the other input to the subtraction circuit, wherein the scaled output of the subtraction circuit forms the accumulator input, wherein the accumulator output is scaled and compared with the instantaneous magnitude of the first-mentioned

subtraction circuit output, wherein if the first-mentioned quantity is less than the second-mentioned quantity the updating of the equaliser coefficients is disabled for four symbol periods and the updating of the canceller coefficients is disabled for one symbol period, and wherein the accumulator output is also scaled and compared with the equaliser coefficient and if found to be the lesser the coefficients of the equaliser are reset to zero.

9. A station as claimed in claim 7, wherein to generate a signal to control the sampling time by a phase-locked loop, the value of the cursor and first post cursor estimates available within the equaliser in each symbol period are added, often having been scaled in a proportion determined from the received signal attenuation, the scaling being determined in combinations with the choice of analogue filtering and digital shaping operation performed on the signal.

10. A station as claimed in claim 3, 4, 5, 6, 7 or 8, wherein the echo cancellation coefficients are generated with the aid of multiplexers via which the accumulators used to generate those coefficients are cross-coupled so that all coefficients can be advanced or retarded one step, wherein said advancing or retarding in combination with the sampling time control circuits of the simulator sample clock, the receive sample clock and the local transmitter symbol clock, permits the echo cancelling functions to track with no discontinuities a continuous frequency difference between the local sampling and transmit clocks, which occurs when the echo simulator clock is not locked to the local transmitter clock.

11. A station as claimed in any one of claims 3 to 10, wherein for "in-service" performance monitoring the relation between the cursor coefficient of the adaptive decision feedback equaliser and the error signal is determined, wherein the frequency with which

a scaled version of the error signal exceeds the cursor coefficient is used as a measure of the error rate, and wherein the mean magnitude of the difference between the cursor coefficient and the error magnitude is used as an absolute measure of the noise margin.

12. A data transmission system substantially as described with reference to the accompanying drawings.

1/9

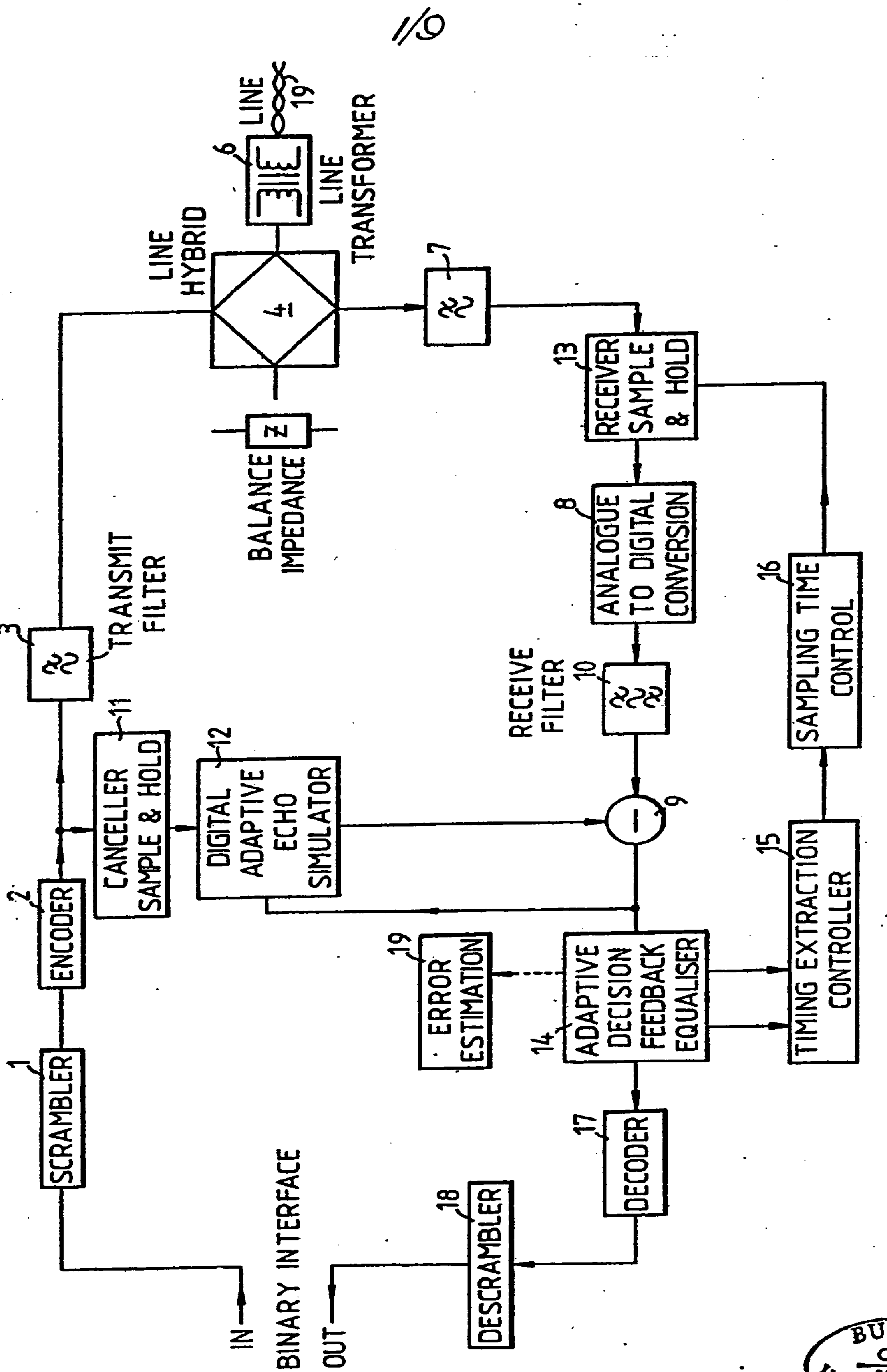
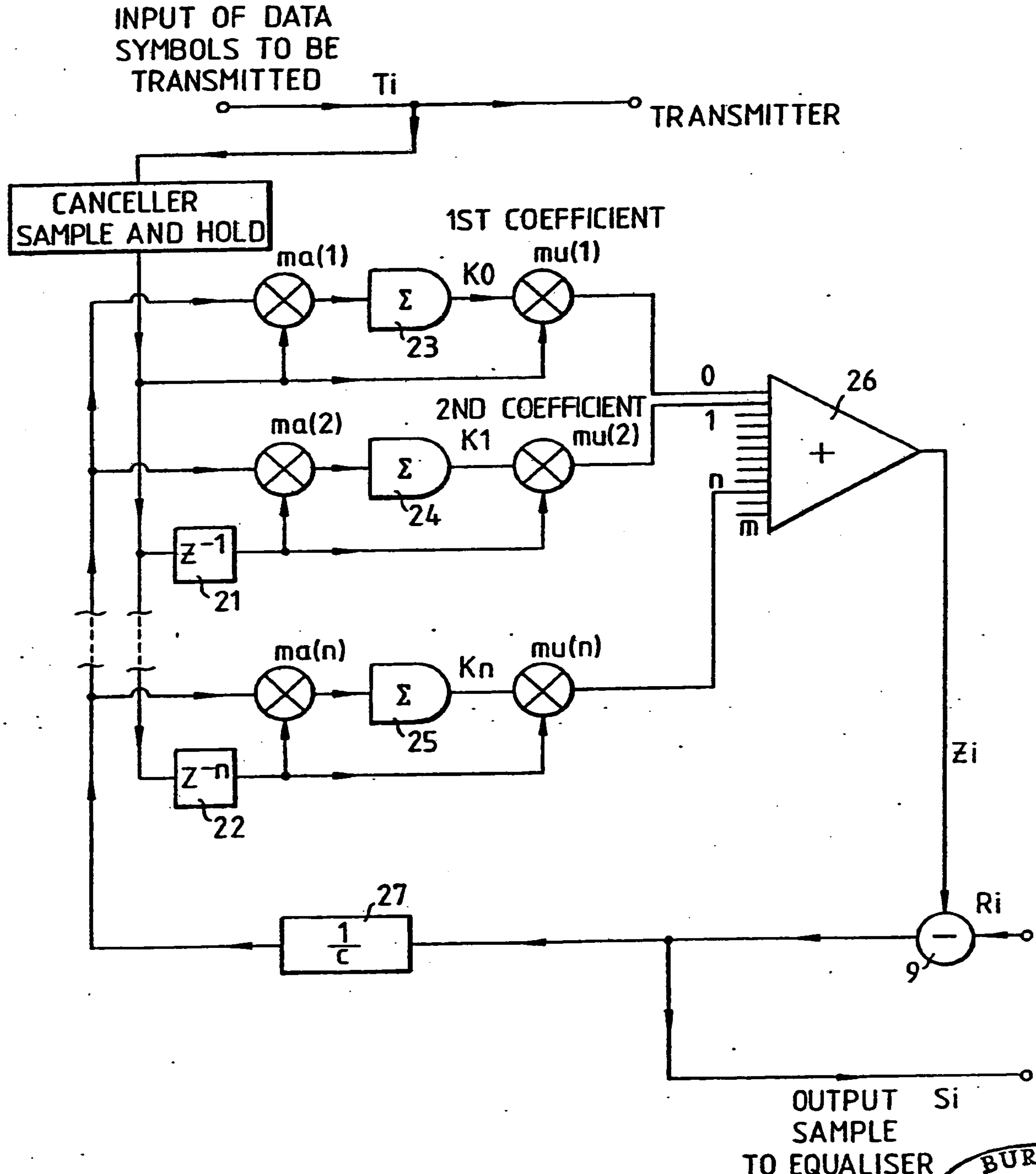

SCRAMBLER
1
ENCODER
2
TRANSMIT FILTER
3
CANCELLER SAMPLE & HOLD
11
DIGITAL ADAPTIVE ECHO SIMULATOR
12
LINE HYBRID
4
LINE TRANSFORMER
6
LINE
19
BALANCE IMPEDANCE
Z
7
RECEIVER SAMPLE & HOLD
13
ANALOGUE TO DIGITAL CONVERSION
8
RECEIVE FILTER
10
9
ERROR ESTIMATION
19
ADAPTIVE DECISION FEEDBACK EQUALISER
14
TIMING EXTRACTION CONTROLLER
15
SAMPLING TIME CONTROL
16
DECODER
17
DESCRAMBLER
18
IN
BINARY INTERFACE
OUT

Fig.1

Fig.2.



INPUT OF DATA SYMBOLS TO BE TRANSMITTED
Ti
TRANSMITTER
CANCELLER SAMPLE AND HOLD
1ST COEFFICIENT
ma(1)
Σ
K0
mu(1)
23
0
26
2ND COEFFICIENT
1
ma(2)
K1
mu(2)
+
24
n
m
Z^-1
21
ma(n)
Kn
mu(n)
25
Zi
Z^-n
22
27
1/c
Ri
9
OUTPUT SAMPLE TO EQUALISER
Si

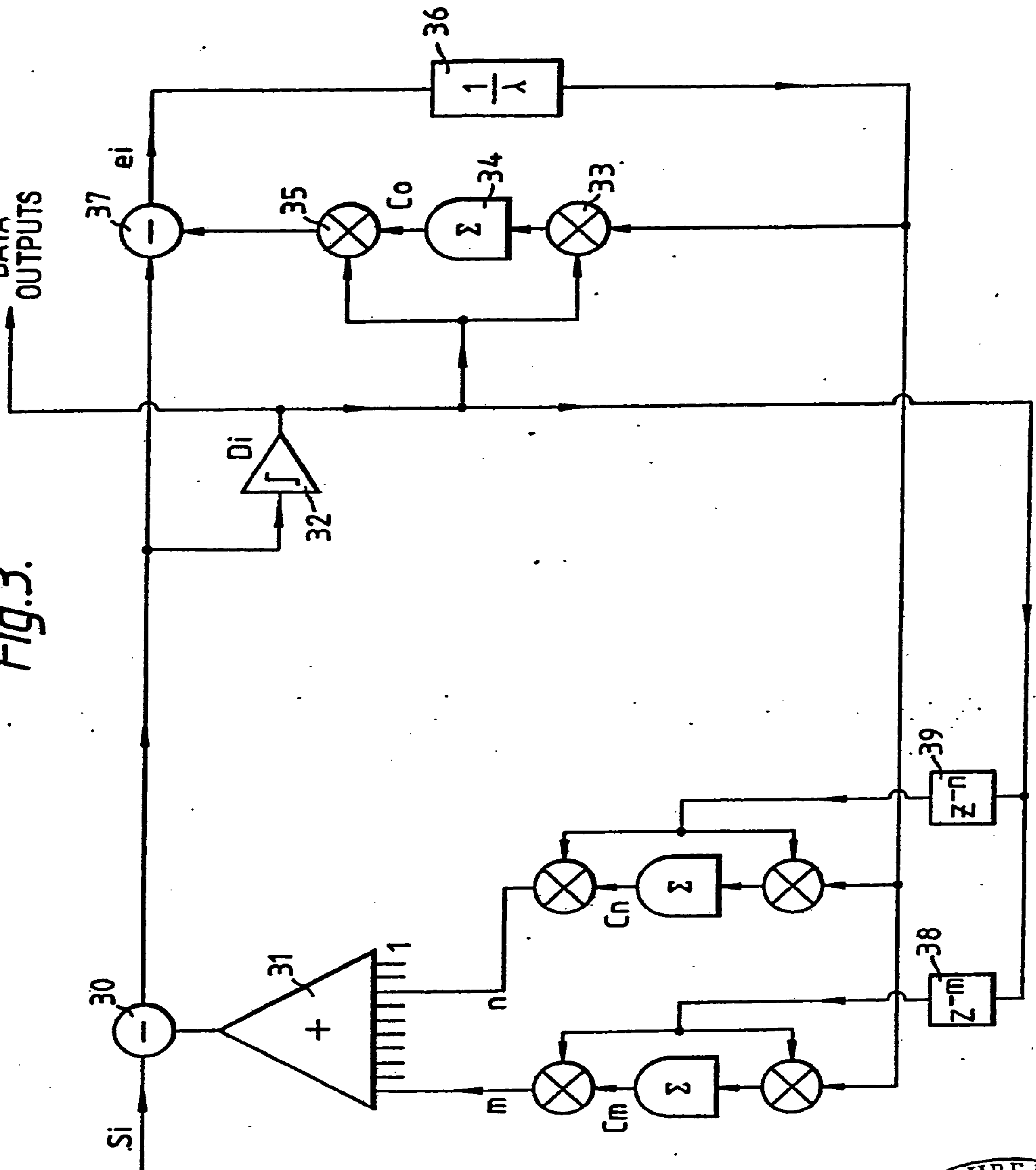

DATA OUTPUTS
Si
30
31
32
33
34
35
36
37
38
39
Di
ei
Co
Cn
Cm
n
m
1
Σ
1/Y
z^{-n}
z^{-m}

Fig.3.

Fig.4.

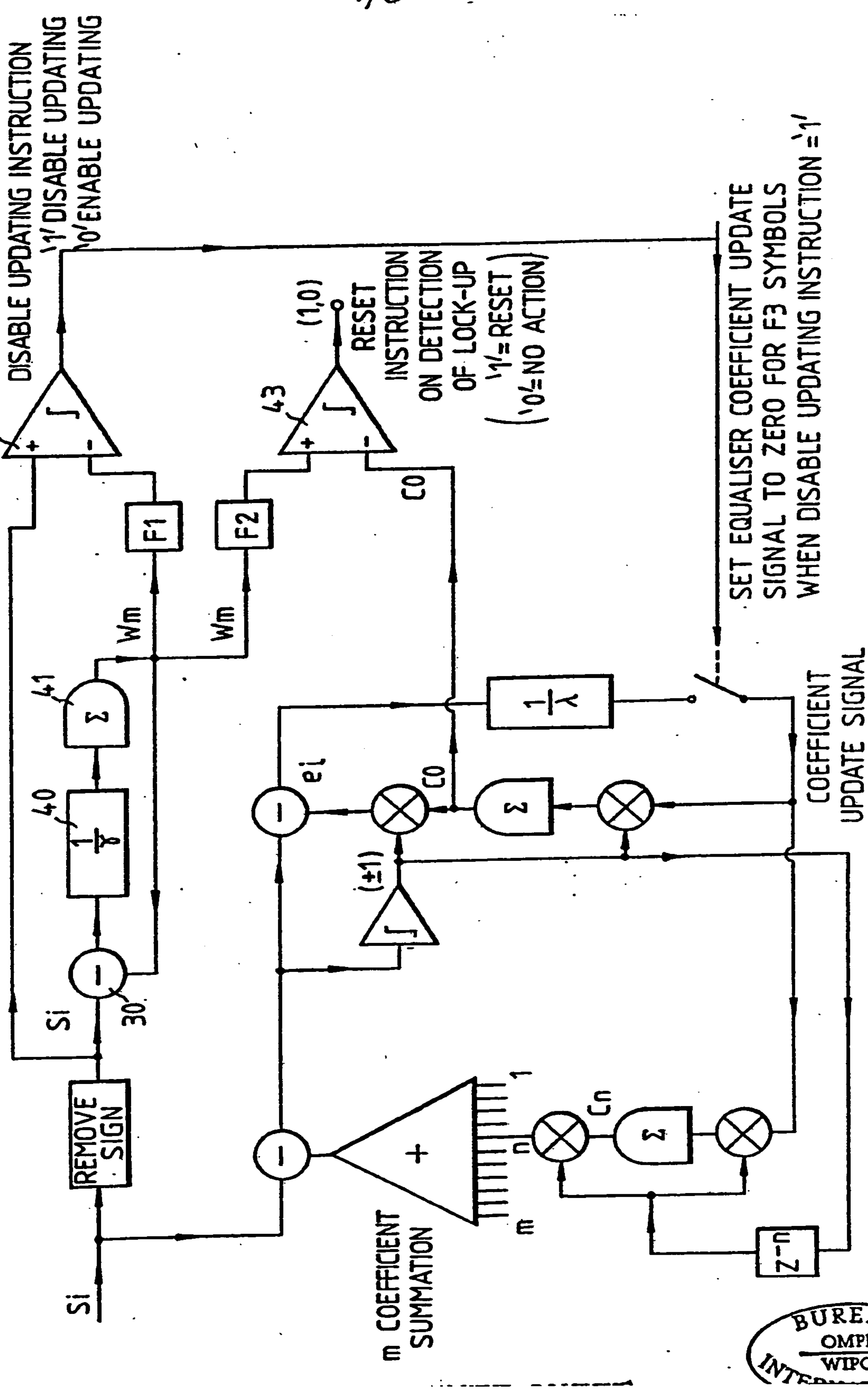
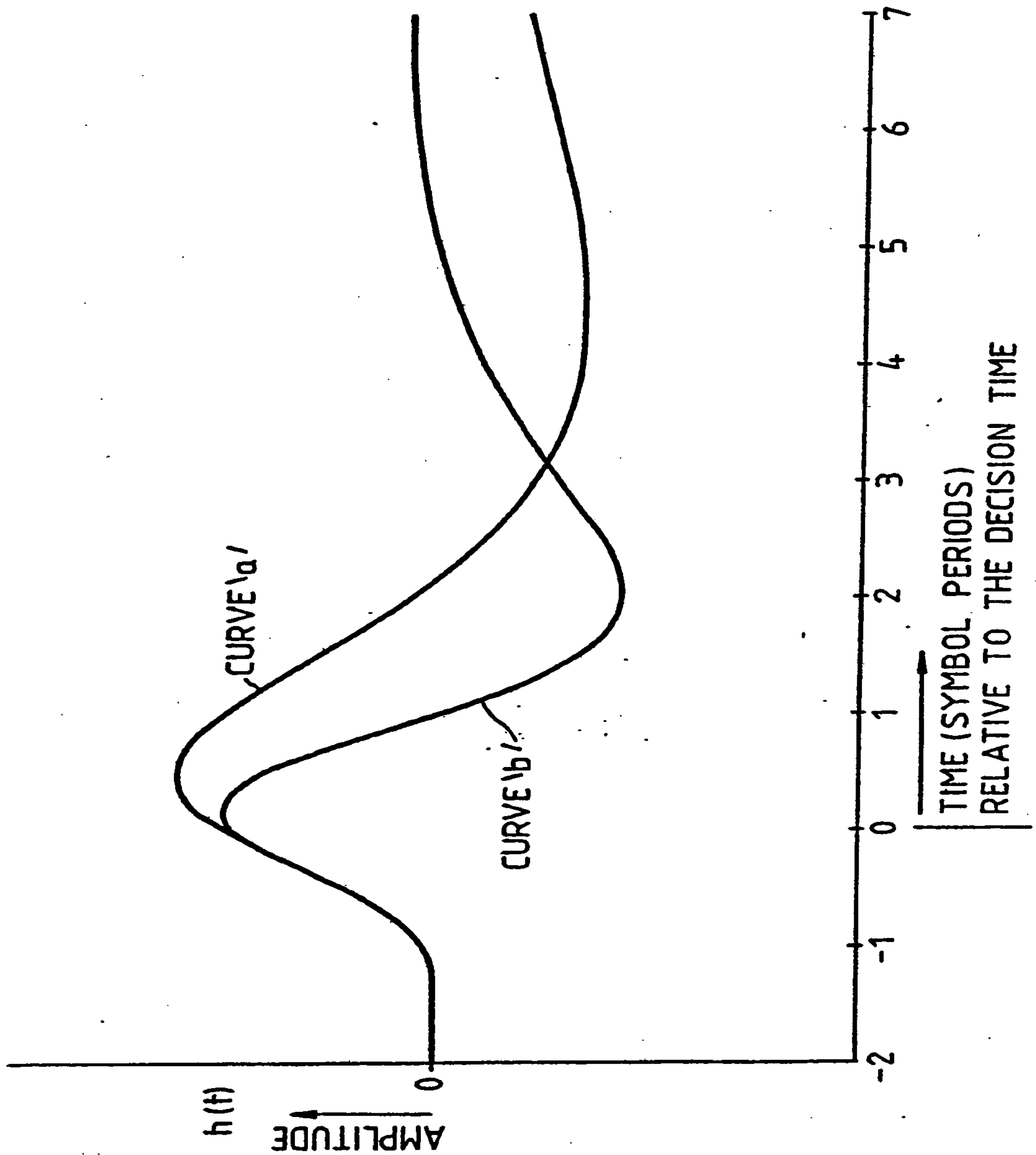

DISABLE UPDATING INSTRUCTION
'1' DISABLE UPDATING
'0' ENABLE UPDATING
42
43
RESET
INSTRUCTION
ON DETECTION
OF LOCK-UP
'1'=RESET
'0'=NO ACTION
(1,0)
F1
F2
C0
Wm
Wm
41
Σ
40
1/γ
Si
30
REMOVE SIGN
Si
ei
(±1)
1/γ
C0
Σ
Σ
Cn
SET EQUALISER COEFFICIENT UPDATE
SIGNAL TO ZERO FOR F3 SYMBOLS
WHEN DISABLE UPDATING INSTRUCTION ='1'
COEFFICIENT
UPDATE SIGNAL
m COEFFICIENT
SUMMATION
m
n
1
Z^{-n}

Fig.5.


CURVE 'a'
CURVE 'b'
AMPLITUDE
h(t)
0
-2
-1
0
1
2
3
4
5
6
7
TIME (SYMBOL PERIODS)
RELATIVE TO THE DECISION TIME

6/9

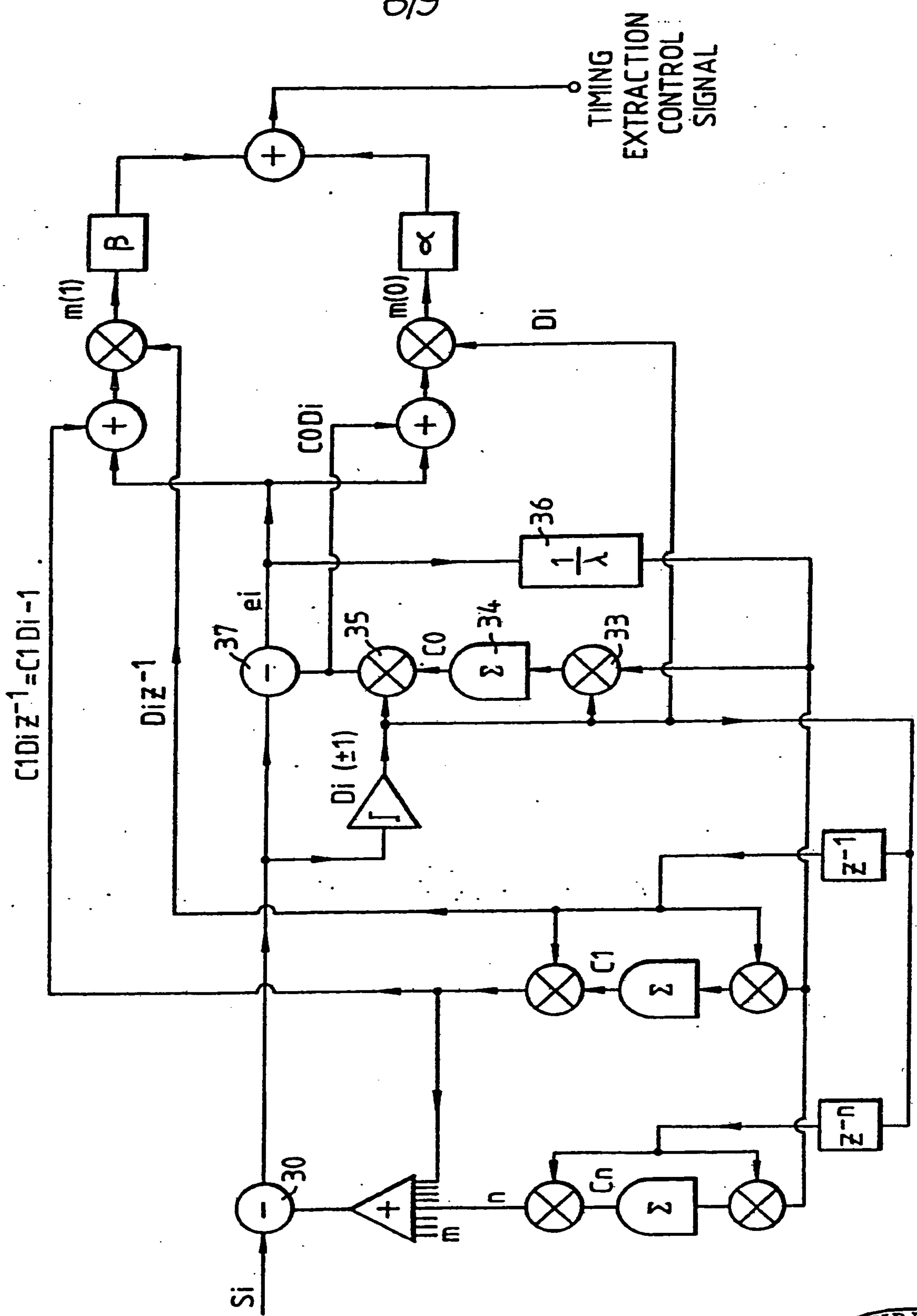
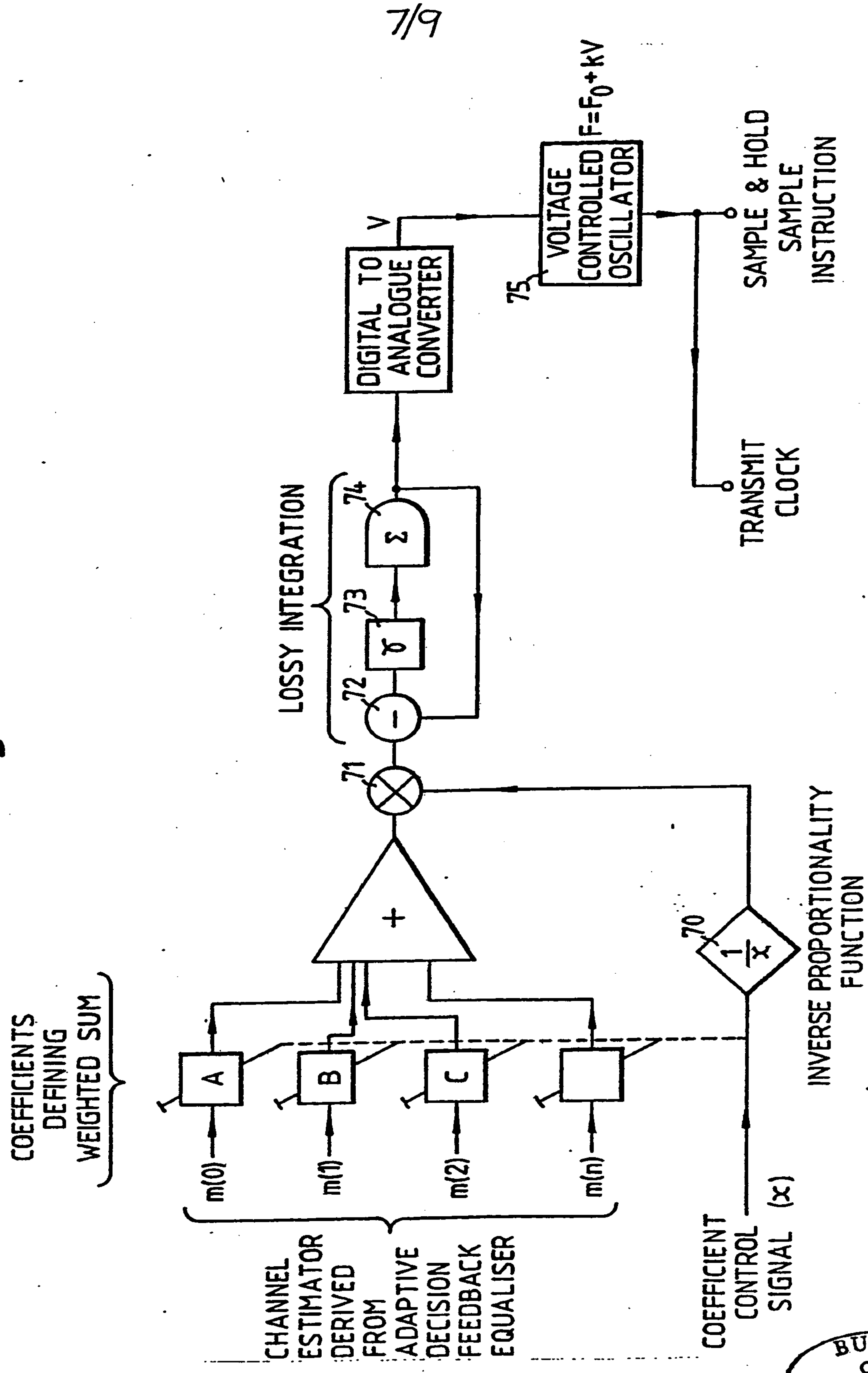

TIMING EXTRACTION CONTROL SIGNAL
β
α
m(1)
m(0)
Di
C0Di
36
1/λ
37
ei
35
C0
34
33
Di (±1)
Di z^-1
C1Di z^-1 = C1 Di -1
C1
Cn
z^-1
z^-n
30
Si
n
m

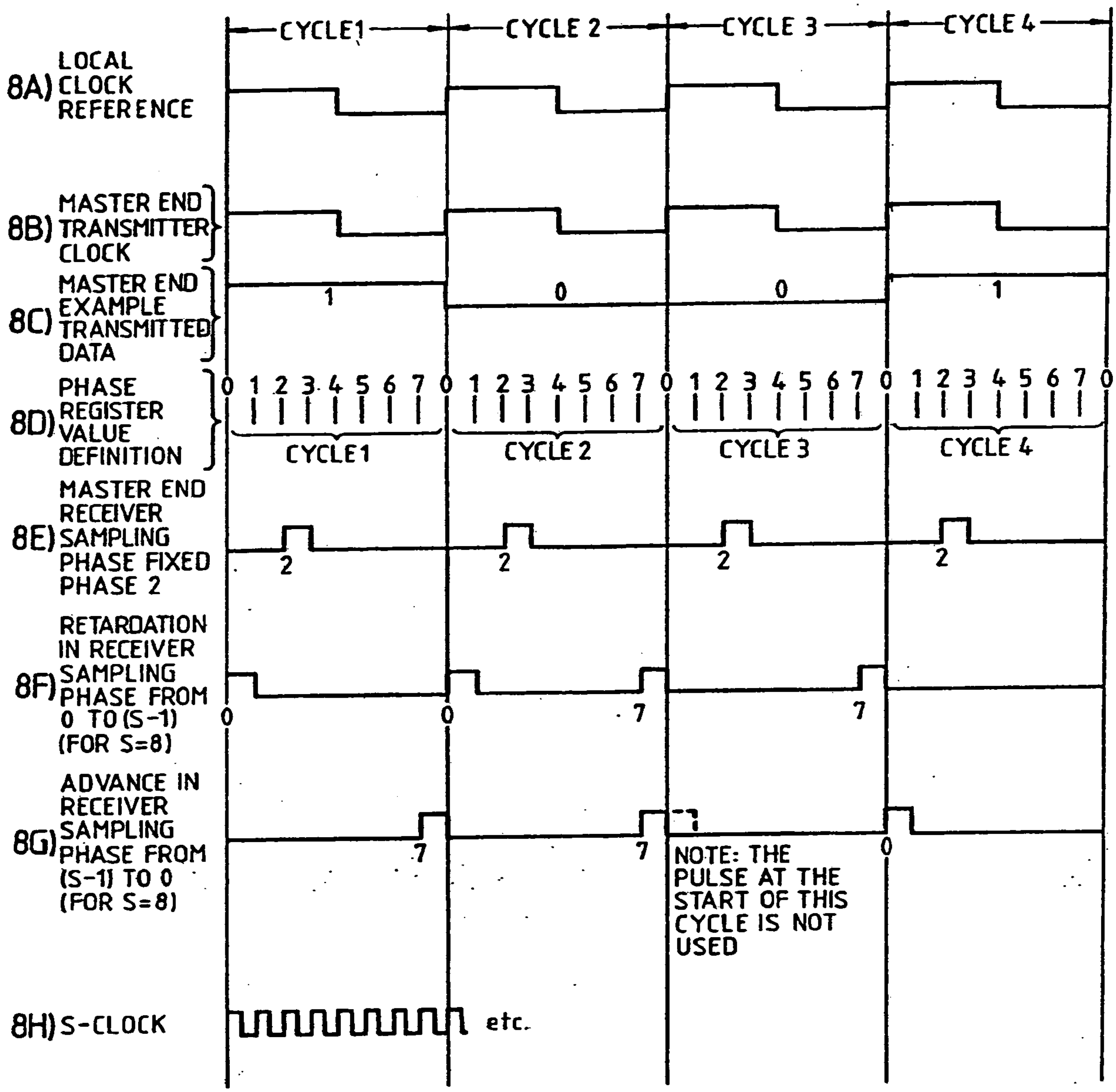
Fig.6.

Fig.7.


COEFFICIENTS DEFINING WEIGHTED SUM
CHANNEL ESTIMATOR DERIVED FROM ADAPTIVE DECISION FEEDBACK EQUALISER
m(0)
m(1)
m(2)
m(n)
A
B
C
+
70
1/x
INVERSE PROPORTIONALITY FUNCTION
COEFFICIENT CONTROL SIGNAL (x)
71
72
73
74
LOSSY INTEGRATION
−
γ
Σ
DIGITAL TO ANALOGUE CONVERTER
V
75
VOLTAGE CONTROLLED OSCILLATOR
F=F0+kV
SAMPLE & HOLD SAMPLE INSTRUCTION
TRANSMIT CLOCK

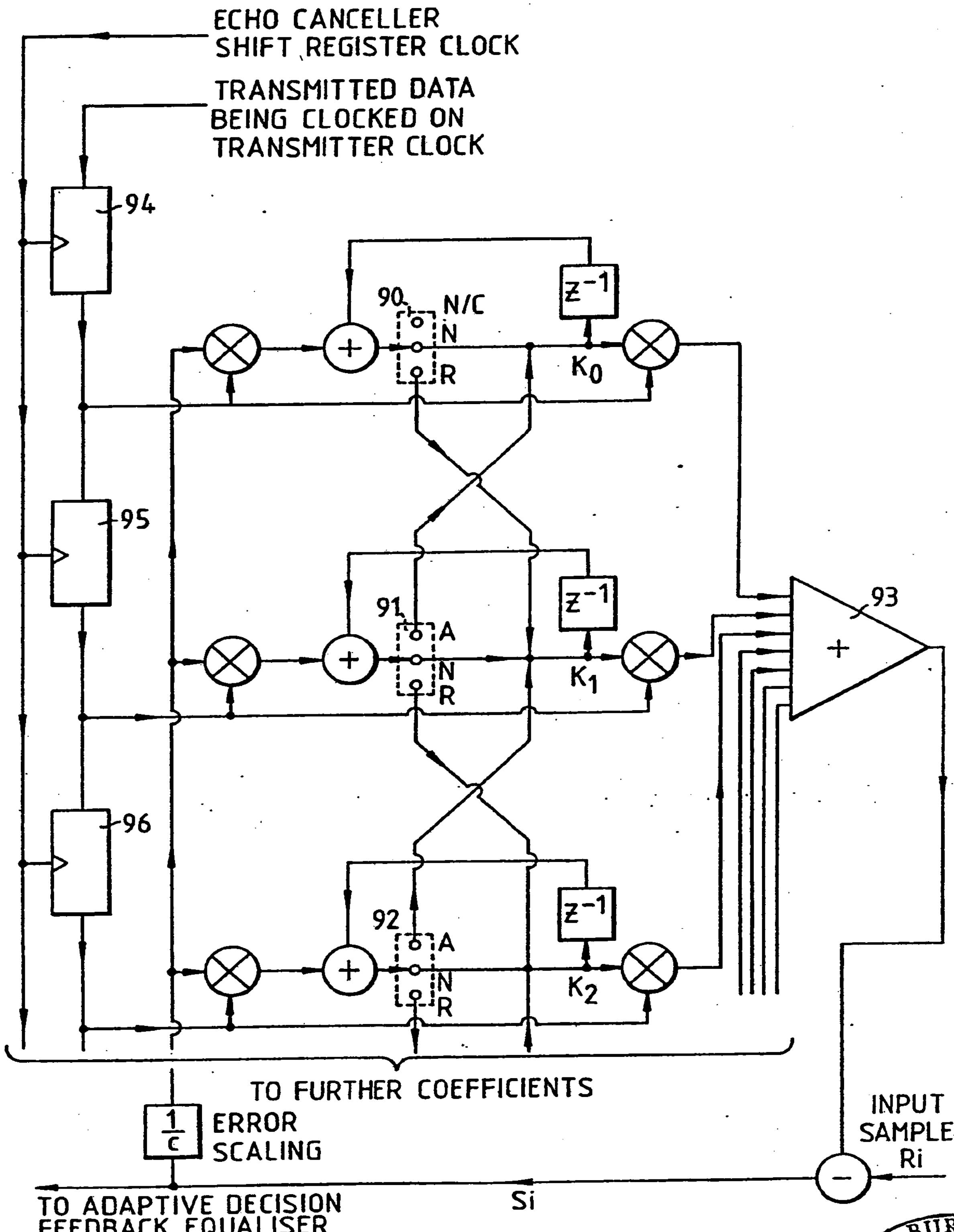
8/9

Fig.8.


CYCLE 1
CYCLE 2
CYCLE 3
CYCLE 4
8A) LOCAL CLOCK REFERENCE
8B) MASTER END TRANSMITTER CLOCK
8C) MASTER END EXAMPLE TRANSMITTED DATA
1
0
0
1
8D) PHASE REGISTER VALUE DEFINITION
0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7 0
CYCLE 1
CYCLE 2
CYCLE 3
CYCLE 4
8E) MASTER END RECEIVER SAMPLING PHASE FIXED PHASE 2
2
2
2
2
8F) RETARDATION IN RECEIVER SAMPLING PHASE FROM 0 TO (S-1) (FOR S=8)
0
0
7
7
8G) ADVANCE IN RECEIVER SAMPLING PHASE FROM (S-1) TO 0 (FOR S=8)
7
7
0
NOTE: THE PULSE AT THE START OF THIS CYCLE IS NOT USED
8H) S-CLOCK
etc.

9/9

Fig.9.


ECHO CANCELLER
SHIFT REGISTER CLOCK
TRANSMITTED DATA
BEING CLOCKED ON
TRANSMITTER CLOCK
94
95
96
90
N/C
N
R
z^{-1}
K_0
91
A
N
R
K_1
93
+
92
A
N
R
K_2
TO FURTHER COEFFICIENTS
$\frac{1}{c}$
ERROR
SCALING
INPUT
SAMPLE
Ri
Si
TO ADAPTIVE DECISION
FEEDBACK EQUALISER

INTERNATIONAL SEARCH REPORT

International Application No PCT/GB 82/00329

I. CLASSIFICATION OF SUBJECT MATTER (If several classification symbols apply, indicate all) [8]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC^3: H 04 B 3/23; H 04 L 25/03

II. FIELDS SEARCHED

Minimum Documentation Searched [4]

Classification System	Classification Symbols
IPC^3	H 04 B 3/23; H 04 L 25/03

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [5]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [14]

Category *	Citation of Document, [16] with indication, where appropriate, of the relevant passages [17]	Relevant to Claim No. [18]
X	National Telecommunications Conference 1978, Conference Record, vol. 2, 3 December 1978 (New York, US) Nielsen et al.: "A digital hybrid for two-wire digital subscriber loops", page 21.2.1-21.2.7, see page 21.2.1, left-hand column, lines 1-12; right-hand column, lines 9-12, line 21 - page 21.2.3, left-hand column, line 12 --	1-6
X	International Conference on Communications, 1981, Conference Record, vol. 2, 14 June 1981 (New York, US) Di Tria et al.: "Design and simulation of a digital DPSK modem for 80 kbits/s full-duplex data transmission on the subscriber loop", pages 25.6.1-25.6.5 see page 25.6.3, left-hand column, lines 3-19 --	1-3
A	IEEE Transactions on Information Theory, vol. IT-17, no. 1, January 1971 (New York, US) Monsen: "Feedback equaliza-	./.

* Special categories of cited documents: [15]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search [2]	Date of Mailing of this International Search Report [2]
28th February 1983	2 1 MARS 1983
International Searching Authority [1]	**Signature of Authorized Officer [20]**
EUROPEAN PATENT OFFICE	G.L.M. Kruydenberg

Form PCT/ISA/210 (second sheet) (October 1981)

International Application No. PCT/GB 82/00329 -2-

III. DOCUMENTS CONSIDERED TO BE RELEVANT (CONTINUED FROM THE SECOND SHEET)		
Category *	Citation of Document, 16 with indication, where appropriate, of the relevant passages 17	Relevant to Claim No 18
	tion for fading dispersive channels", pages 56-64, see page 61, left-hand column, lines 25-30	6,7
	--	
A	Patents Abstracts of Japan, vol. 5, no. 66, see page E55,738, JP, A, 56-17532 (Nippon Denki) 2 May 1981	8

Form PCT ISA/210 (extra sheet) (October 1981)